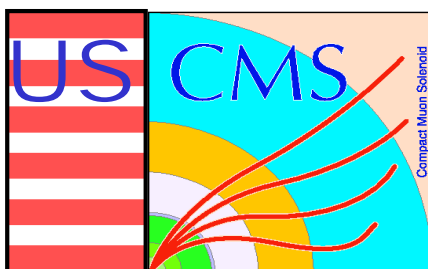


# ***WBS 1.2***

## ***EMU Electronics***



**T.Y. Ling**

***DOE/NSF Review, May 9, 2001***



# ***Outline***

- **System Overview**
- **Status, Schedule, Cost**
- **Technical Progresses**
- **Conclusion**



# ***Functions of Electronics***

- **Acquire precise muon data for off-line analysis**
  - Cathode strips: precise **azimuthal (bending) position** in each layer by interpolation of induced strip charges.
  - Anode wires: precise **timing** and coarse **radial position**.
- **Generate primitives for Level-1 Trigger**
  - Identify **Local Charged Track** segments using cathode and anode signals



## ***Front-end Requirements***

- **Cathode**
  - Low Noise:  $< 25 \text{ e's/pF}$
  - Shaper peaking time: 100 ns
  - Digitization precision: 12-bit
  - Dynamic range:  $> 16 \text{ MIPs}$
  - Non-linearity:  $< 1\%$  over full range
  - Calibration precision:  $< 1\%$  over full range
- **Anode**
  - Low Noise: 0.5 fC @ 0 pF; 1.7 fC @ 200 pF
  - Shaper peaking time: 30 ns
  - Two threshold discriminator
  - Time slew: 3 ns

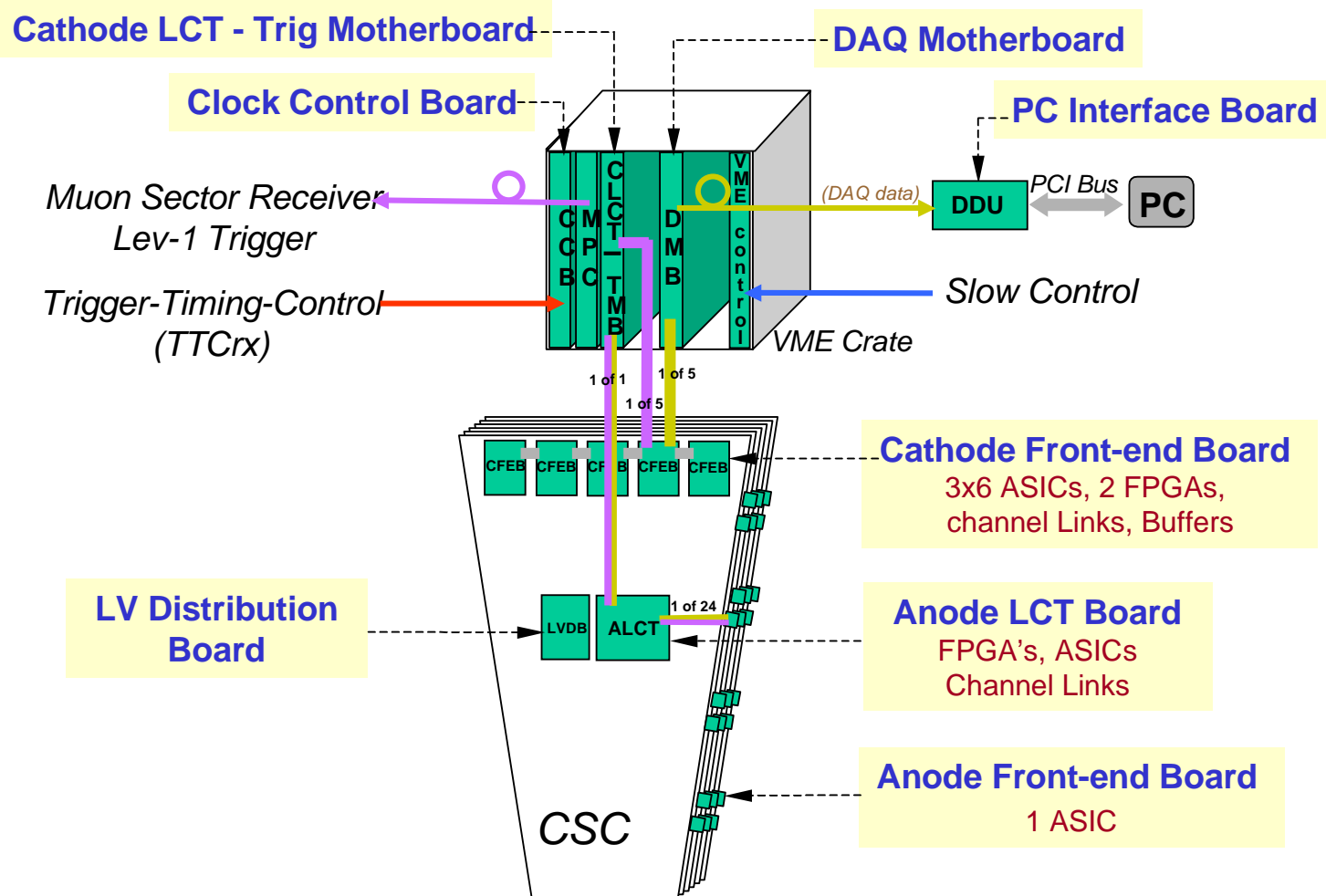


# *Trigger Requirements*

- **Cathode LCT**
  - Identify cathode track segment and use angle of segment for  $P_t$  trigger
  - For  $P_t$  threshold of 20-40 GeV requires  $\Delta p/p < 30\%$  (in order to limit single muon trigger rate in Level-1 to a few KHz)
  - Track hits must be located to within  $\frac{1}{2}$  strip width in each chamber layer
- **Anode LCT**
  - Form cathode track segment.
  - Tag bunch crossing of track segment with  $\geq 92\%$  efficiency per chamber



# System Layout





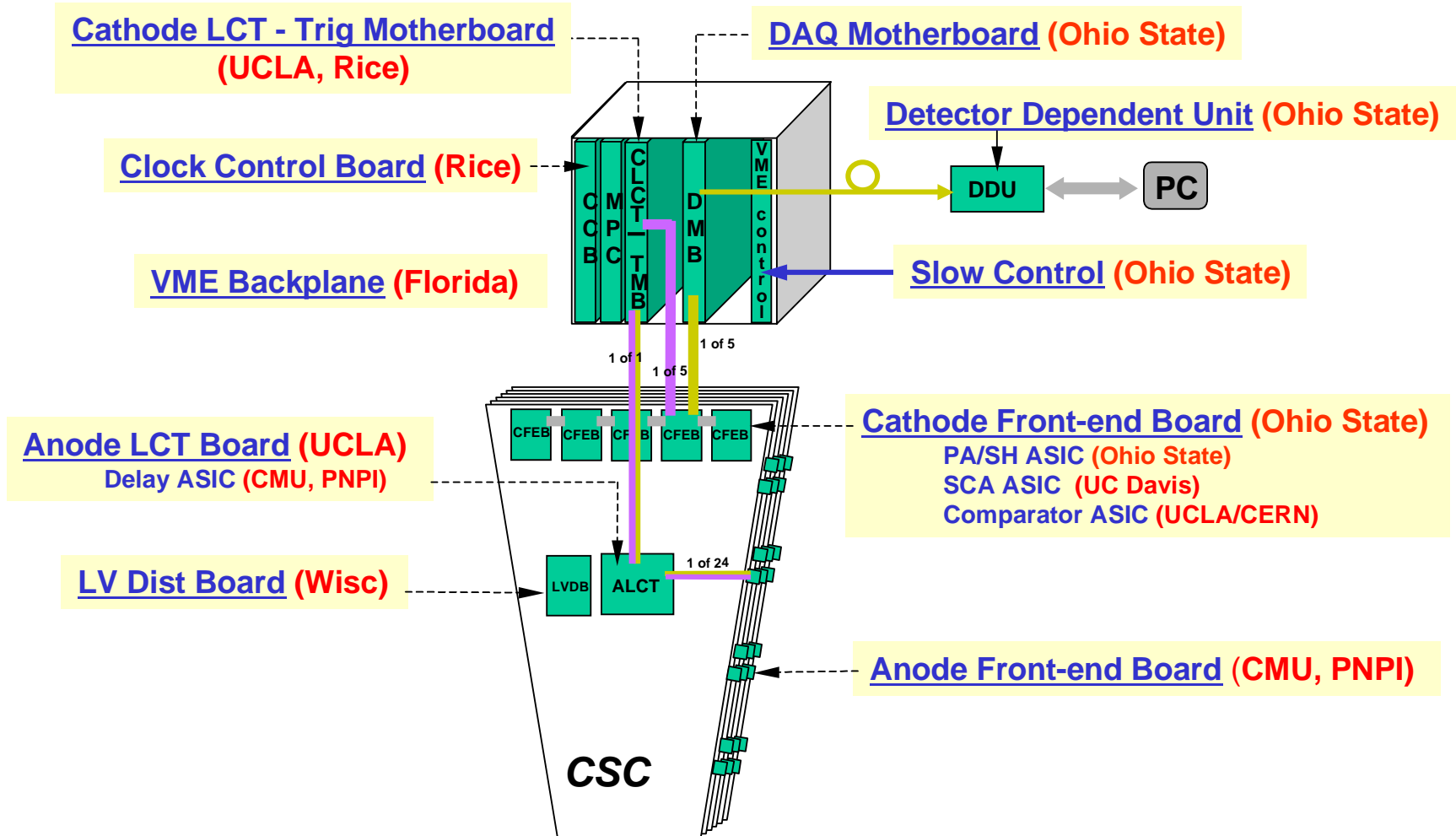
## ***Baseline Scope***

<b>96ch Cathode Front-end Board</b>	<b>1900* boards + cables</b>
<b>16ch Anode Front-end Board</b>	<b>9742* boards + cables</b>
<b>Anode LCT Board (1 board / CSC)</b>	<b>396* boards + cables</b>
<b>DAQ-Motherboard (1 board / CSC)</b>	<b>396* boards + links</b>
<b>Detector Dependent Unit (DDU)</b>	<b>33* boards (9U)</b>
<b>Cathode LCT /TRIG-MB (1 board /CSC)</b>	<b>396* boards + cables</b>
<b>Clock Control Board (1 board/ Crate)</b>	<b>66* boards</b>
<b>Low Voltage Distribution Boards</b>	<b>396* boards + cables</b>
<b>Low Voltage Supply System</b>	

*\* numbers include 10% spare*

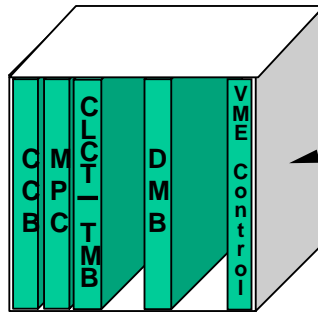


# Institutional Responsibilities

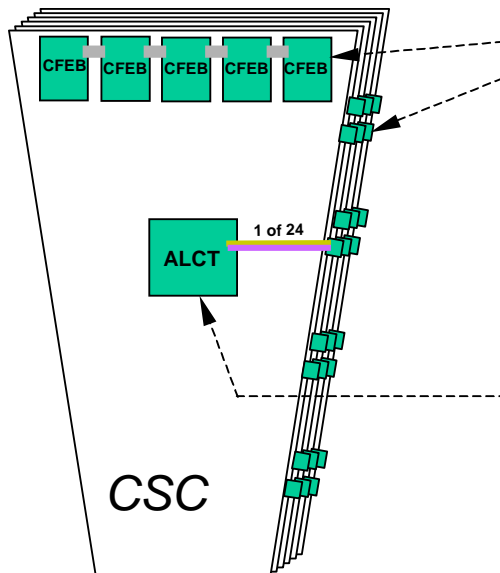




# Schedule in EMU Project File



3/1/01	VME Back-plane ready
3/1/01	New Prototype Boards Ready
3/1/02	Final Prototype Boards
10/1/02	Begin Production
9/30/04	Finish production



## CFEB & AFEB

10/1/00	Start procurement (ASIC, components)
1/4/01	Begin Board production
5/18/01	Deliver first batch of prod. Boards
9/30/03	Finish production

## ALCT

6/11/01	Deliver Final Prototype
9/27/01	Pre-production boards ready
10/1/01	Begin production
9/30/03	Finish production



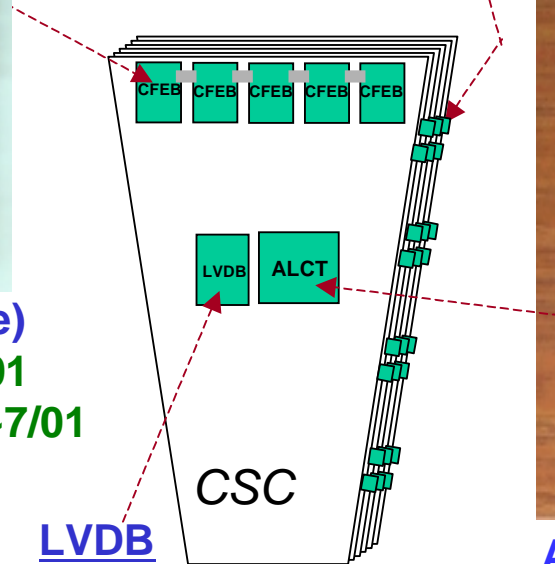
# Status: On-Chamber Boards



**CFEB (Final Prototype)**  
 Production started 2/01  
 Deliver first 120 boards ~7/01



**A FEB (Final Prototype)**  
 Production started 2/01  
 Deliver first 600 boards 6/01



**LVDB**  
 Design finalized.  
 Start production 7/01(?)



**ALCT (Next to final prototype)**  
 Final prototype by 7/01  
 Pre- production board 10/01



## CFEB Production Cost (M&S)

*For baseline scope: 1900 boards*

	Budget (\$)	Actual (\$)	
		Committed	Need to finish
Preamp/Shaper	386,254	343,000	
Switched Capacitor Array	511,987	448,000	
Comparator	255,170	172,000	
ADC	208,467	211,748	
FPGA	149,765	27,101	66,000
Other components	584,370	542,840	40,000
ST Regulators			19,000
pc boards	515,270	120,565	5,000
board assembly	190,101	139,812	5,000
Signal Cables (from CSC)	187,346	146,897	
Inter-CFEB Cables	26,918	7,544	
<b>Total</b>	<b>3,015,648</b>	<b>2,159,507</b>	<b>135,000</b>



## ***AFEB Production Cost (M&S)***

*For baseline scope: 9742 boards*

	<b>Budget (\$)</b>	<b>Actual Committed (\$)</b>
Preamp/Shaper/Discriminator	212900	215000
Delay Chip		93000
other components	97419	79000
pc boards	31176	8000
board assembly	97419	58000
AFEB to ALCT cables	286682	298000
<b>Total</b>	<b>725,596</b>	<b>751,000</b>



## ***Progresses: On-chamber Boards***

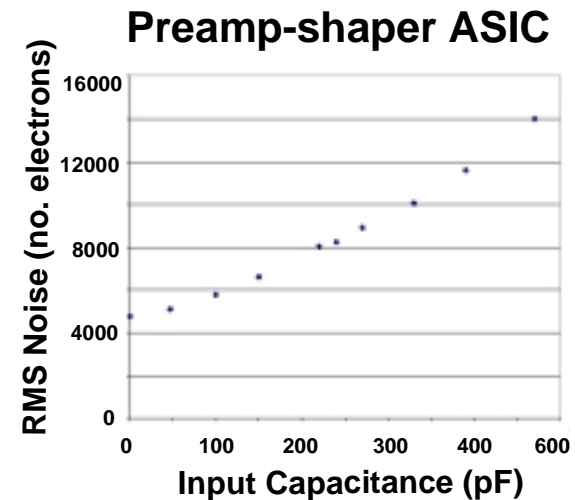
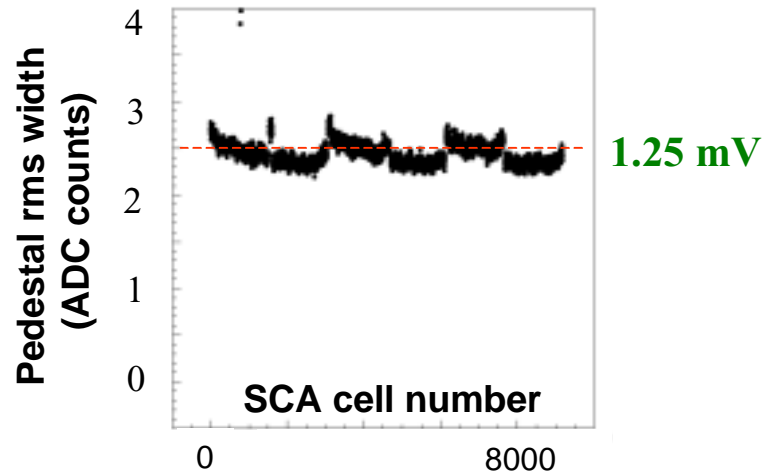
- Integrated electronics system successfully tested with CSC prototype at GIF, CERN (8/99).
- CFEB, AFEB design performance achieved.
- First on-chamber ALCT prototype board produced (3/00) and tested (5/00).
- Radiation tolerance tests for all on-chamber prototype boards (6/00).
- Magnetic field tolerance tests (8/00).
- AFEB layout finalized (9/00)
- Spark protection circuits added on CFEB and tested. Layout of CFEB finalized. (12/00).



# Cathode Front-end Board

Gain	0.83 mV/fC
Linearity	0.6%, 0 - 1.7 V
Dynamic range	0 - 18 MIP
System “noise”	1.25 mV ( <i>rms</i> )

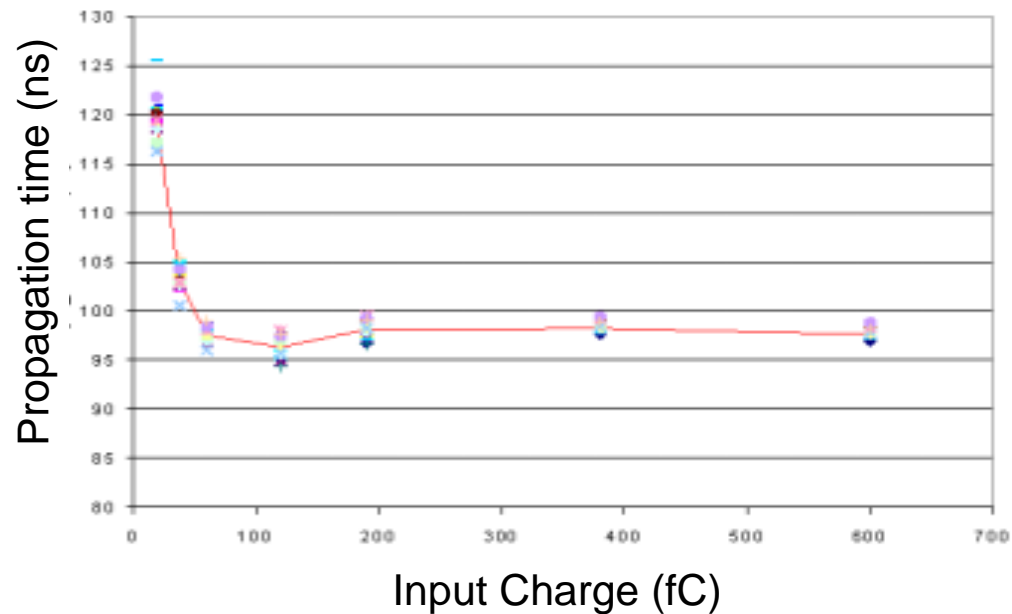
*Includes Pre-Amp noise, SCA pedestal variation, plus all other on-board noise.  
Measured with CFEB mounted on full-size CSC chamber.*





# Anode Front-end Board

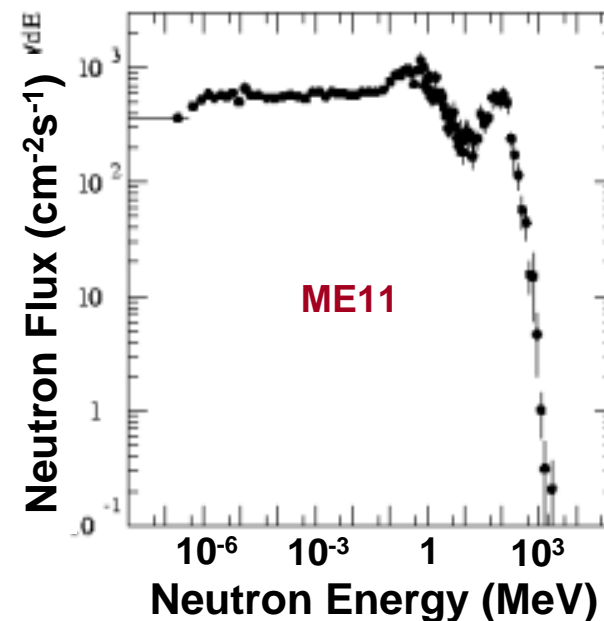
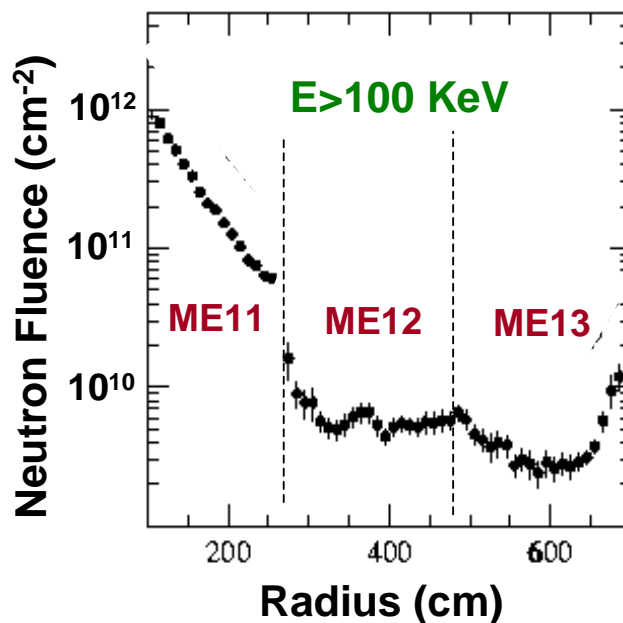
<b>Amp Gain</b>	<b>6.5 mv/fC</b>
<b>Min Threshold</b>	<b>7 fC @ 180 pF</b>
<b>Slewing time</b>	<b>3 ns</b>





# LHC Radiation Background

- **Radiation Levels in EMU** (*M. Huhtinen*)  
*Integrated over 10 LHC years ( $5 \times 10^7$  s at  $10^{34}$  cm $^{-2}$ s $^{-1}$ )*
  - **Neutron Fluence (>100 keV):**  $(0.02 - 6) \times 10^{11}$  cm $^{-2}$
  - **Total Ionizing Dose:**  $(0.007 - 1.8)$  kRad





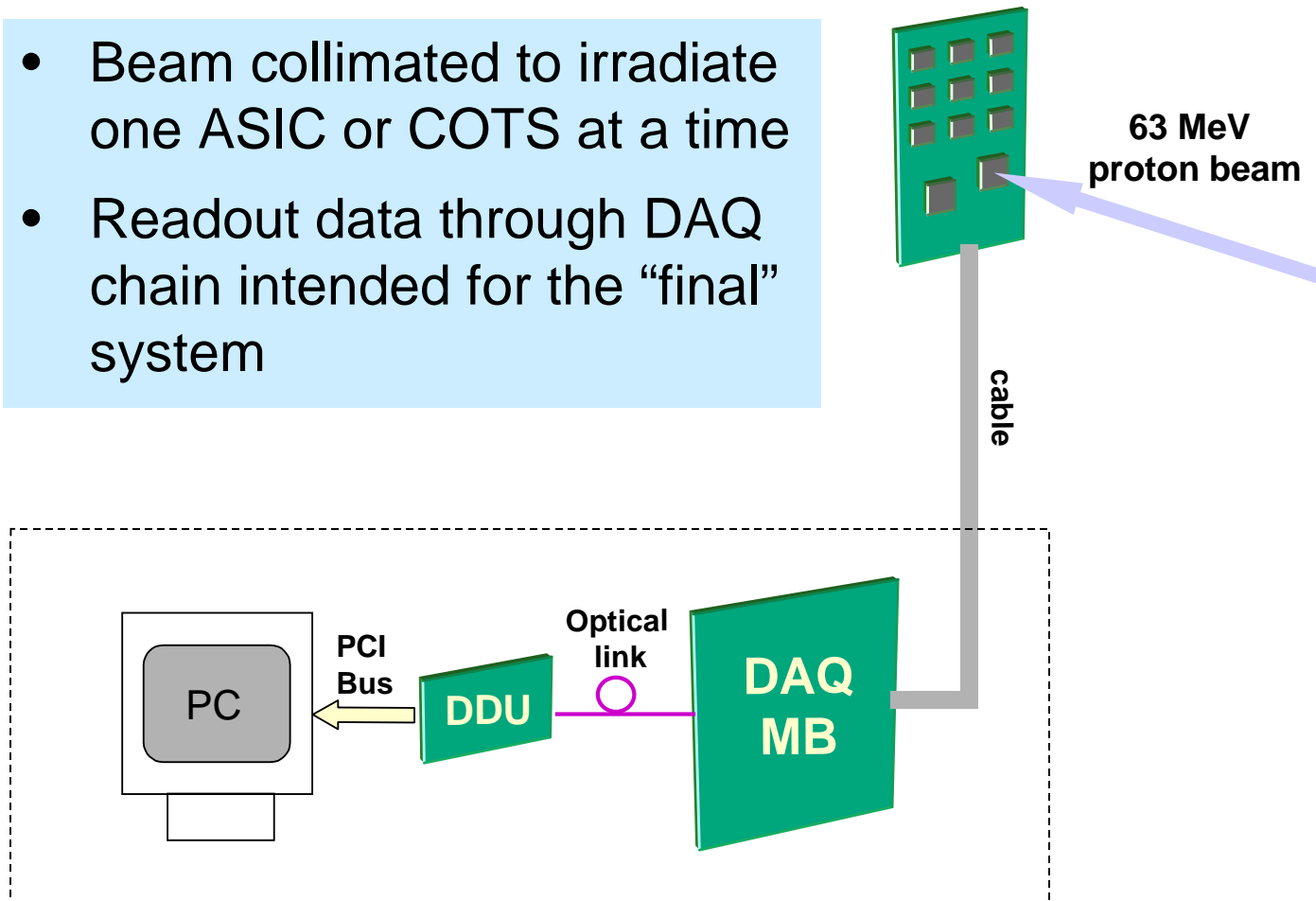
## ***Radiation Tolerance Tests***

- Measured Single Event Effect (SEE) and Total Ionization Dosage (TID) effect with 63 MeV proton beam. (At UC Davis, 4-6/2000)
- Measured effects due to Displacement damage of bipolar and biCMOS w/ 1 MeV neutrons (At OSU, 4-6/2000)
- Results:
  - Negligible degradation of analog performance due to TID ( $>10$  Krad) or displacement ( $2 \times 10^{12}$  cm<sup>-2</sup> neutrons)
  - No latch-ups observed up to proton fluence of  $2 \times 10^{12}$  cm<sup>-2</sup>
  - SEU in FPGA's observed and Cross sections measured. All SEU's recoverable by reloading FPGA's. SEU rate at peak LHC lumi manageable for CFEB, but higher for ALCT.



# Radiation Test Setup

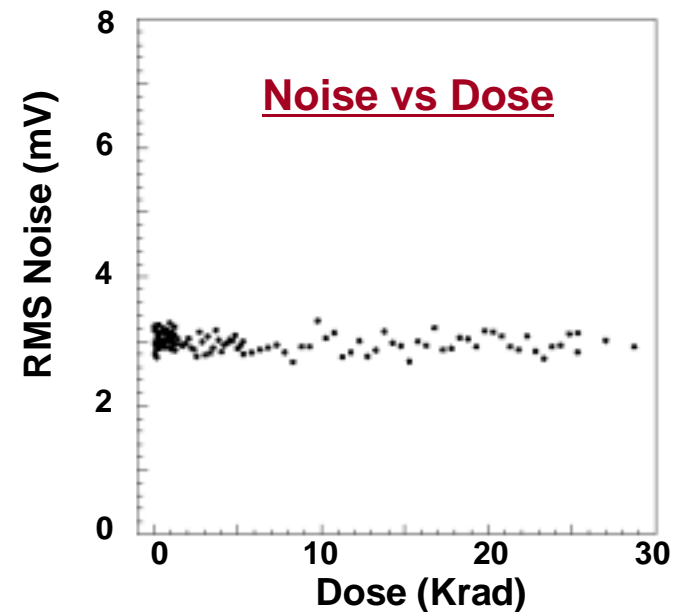
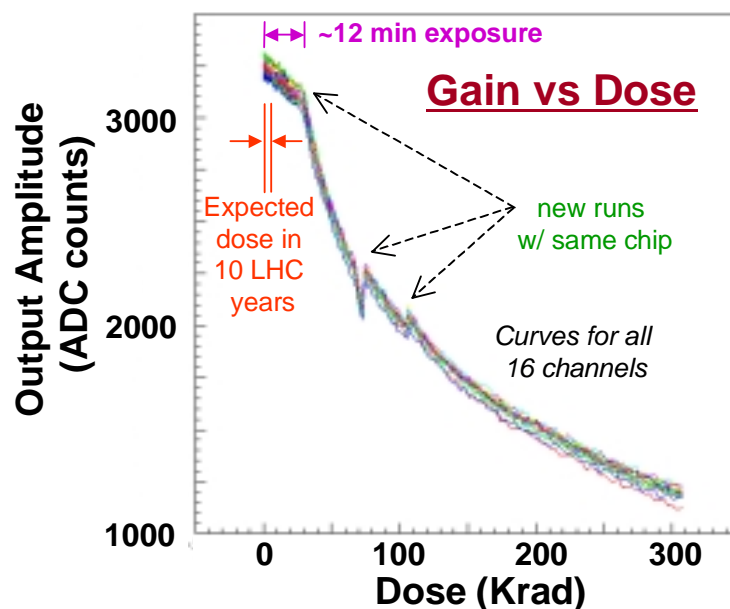
- Beam collimated to irradiate one ASIC or COTS at a time
- Readout data through DAQ chain intended for the “final” system





## Preamp-Shaper ASIC

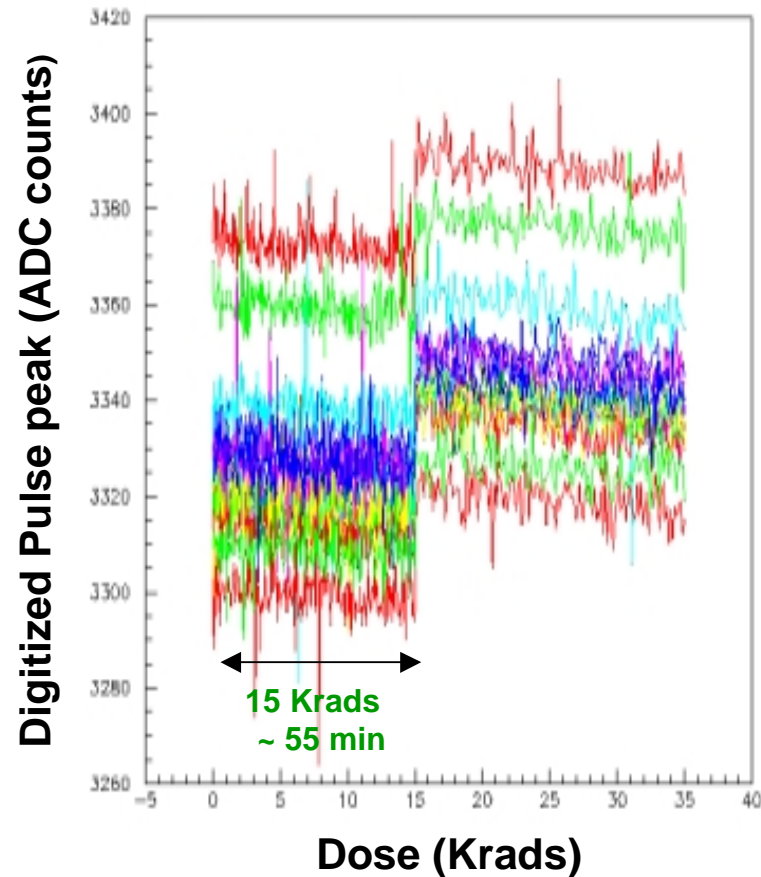
- No single event latch-up for proton fluence of  $2.28 \times 10^{12} \text{ p/cm}^2$
- No shift register errors
- Gain decreases by factor of 2.8, from 0-300 Krad (~ 2 hr run). Not a problem at LHC rates.
- No change in amplifier noise 0-30 kRad.





## Switched Capacitor ASIC

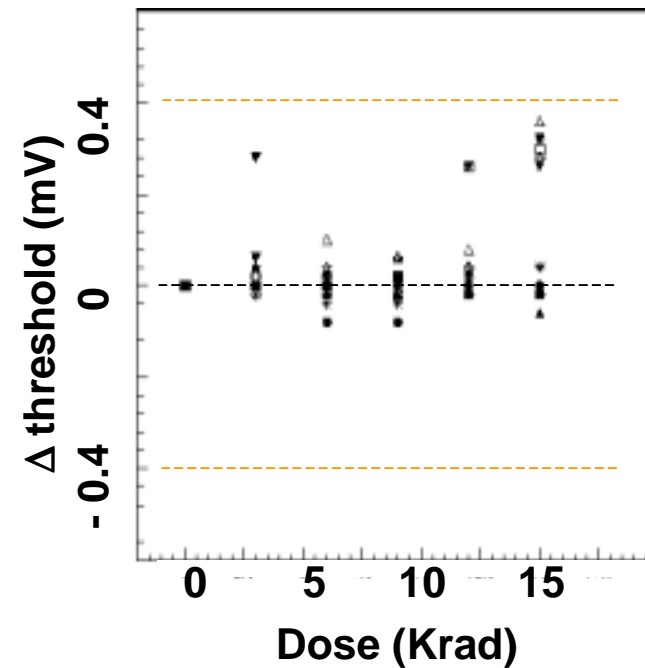
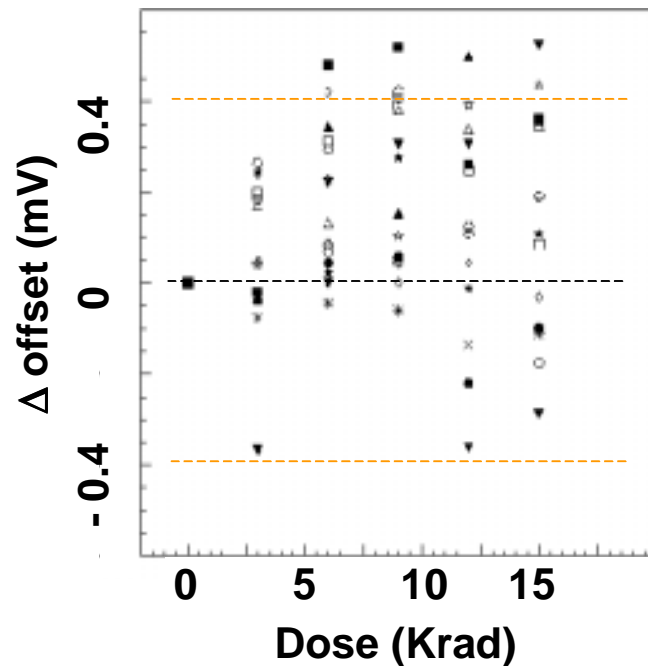
- No single event latch-up for proton fluence of  $1.7 \times 10^{12} \text{ p/cm}^2$
- No degradation of analog performance
- Slight decrease in digitized pulse height vs dose due to output amp gain drop. Not a problem at LHC rates
- Negligible change in noise and pedestal 0 -10 kRad





## Comparator ASIC

- No single event latch-up for proton fluence of  $1.1 \times 10^{12} \text{ p/cm}^2$
- Shift of thresholds and offsets  $< 0.4 \text{ mV}$





## Summary of SEU Measurements

Device (Function)	Proton Fluence ( $10^{11} \text{ cm}^{-2}$ )	Dosage (kRad)	Number of SEU's	SEU Xection ( $10^{-10} \text{ cm}^2$ )
XILINX Spartan XCS30XL (Readout Controller)	1.0	13.4	27	2.7
XILINX Spartan XCS30XL (Multiplexer)	2.9	38.1	34	1.2
XILINX CPLD XC9536XL (Chip 1)	2.8	37.8	106	3.8
XILINX CPLD XC9536XL (Chip 2)	3.1	41.3	117	
XILINX Virtex XCV50 (Readout Controller & MUX)	0.9	12.5	16	1.7
Altera Chip on ALCT	1 SEU / proton fluence of $4.4 \times 10^8 \text{ cm}^{-2}$			23

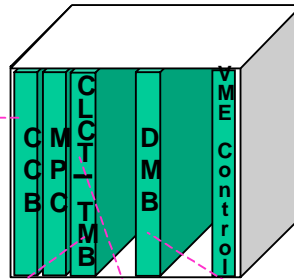


## **Status: Off-Chamber Electronics**

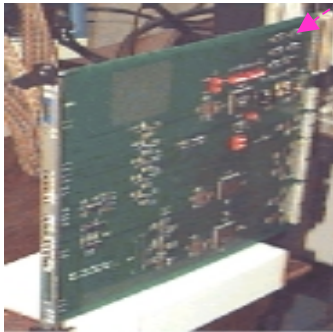
**First Prototype Boards produced and tested (8.99)**



CCB-99



DDU-99



TMB-99



CLCT-99

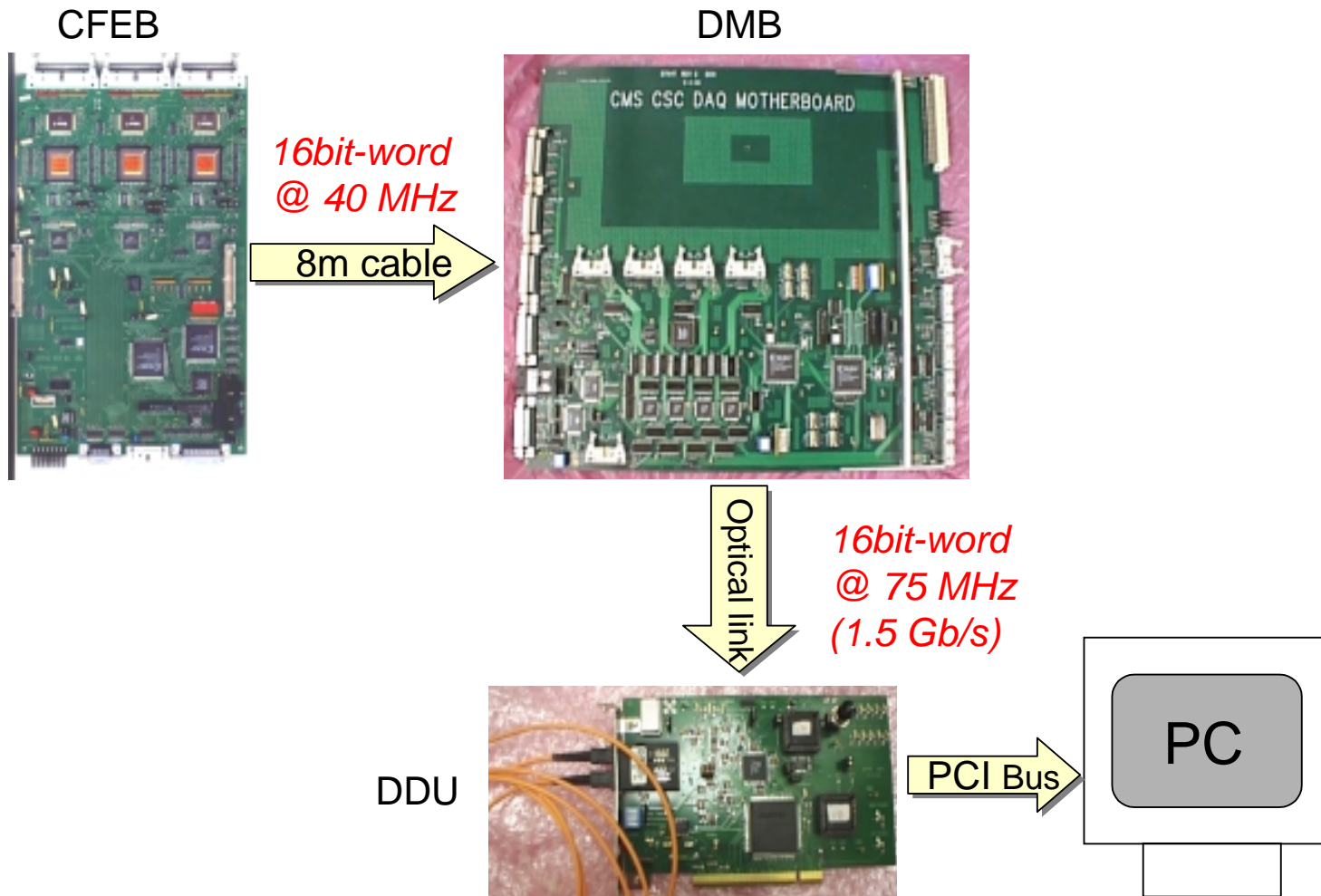


DMB-99

**Next Prototype Boards in progress.**



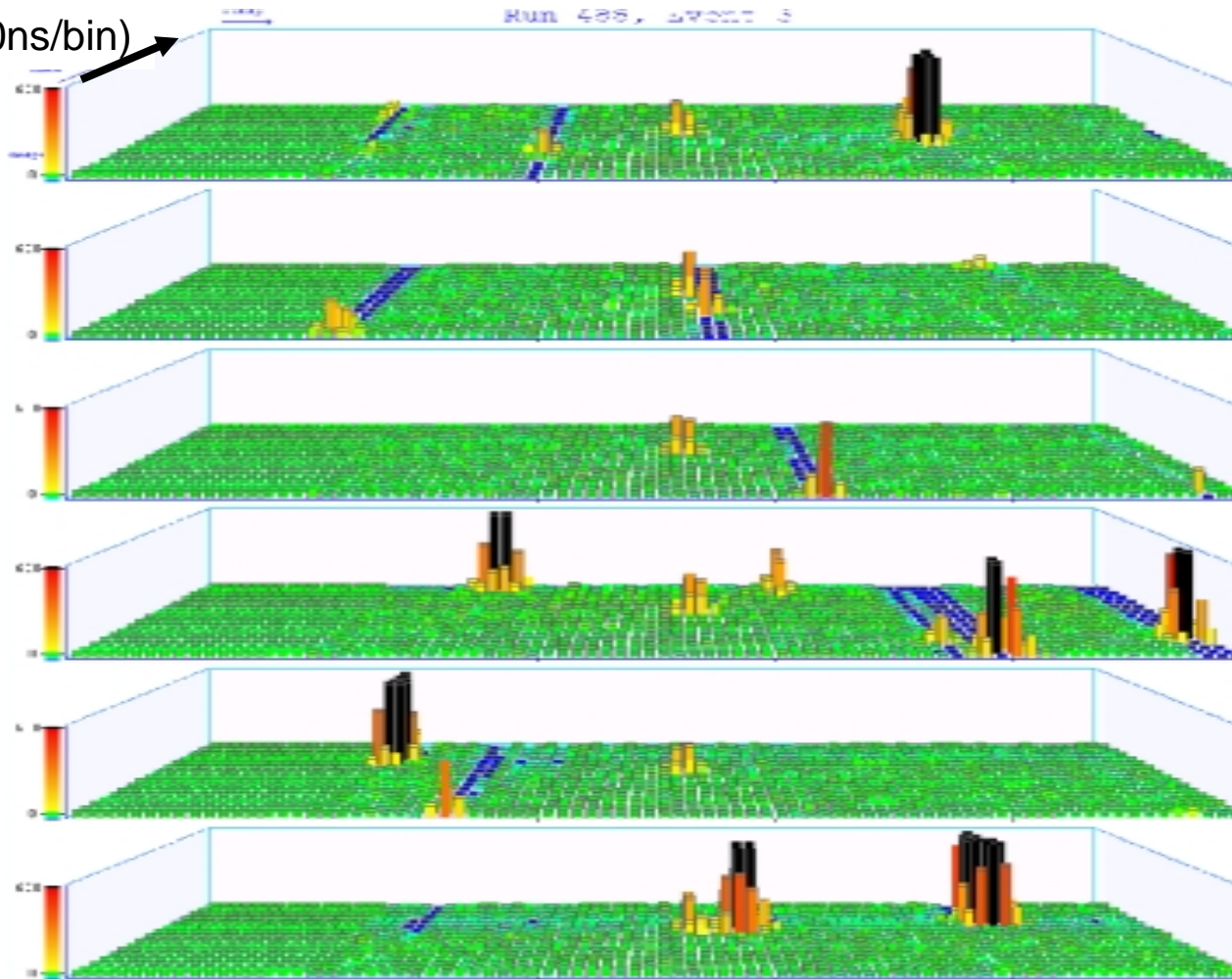
# Integrated System Test (8/99)





## Event from X5 Beam test (8.99)

Time (50ns/bin) →



Source  
strength  
 $K=5$

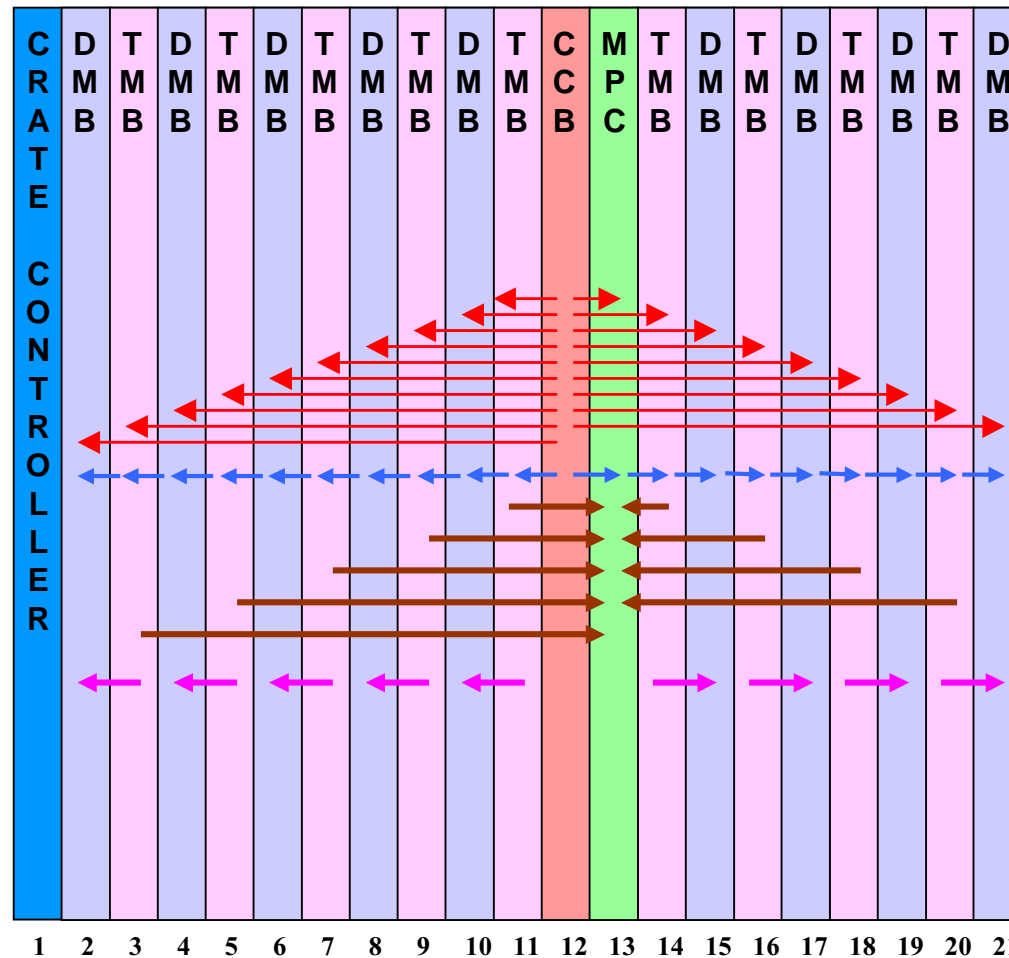


## ***Progresses: Off-chamber Boards***

- **Specifications of and inter-connections between DMB, TMB, and CCB) determined. (2/01)**
- **Custom VME Backplane**
  - Use GTLP @ 80 MHz (replaces channel links in trigger path)
  - Design finished. Full size backplane (21 slots) ordered (4/01)
- **New DAQ Motherboard Prototype (DMB-01)**
  - New prototype design, schematics and layout finished (3/01)
  - Partially assembled board under tests (5/01)
- **New Trigger Motherboard +CLCT Prototype (TMB-01)**
  - Schematics nearly finished (4/01). Layout will be done in 5/01.
- **New Clock Control Board Prototype (CCB-01)**
  - Mezzanine card (TTCrx) schematics finished (4/01)
  - Layout of CCB finished (4/01)



# Peripheral VME Crate Organization



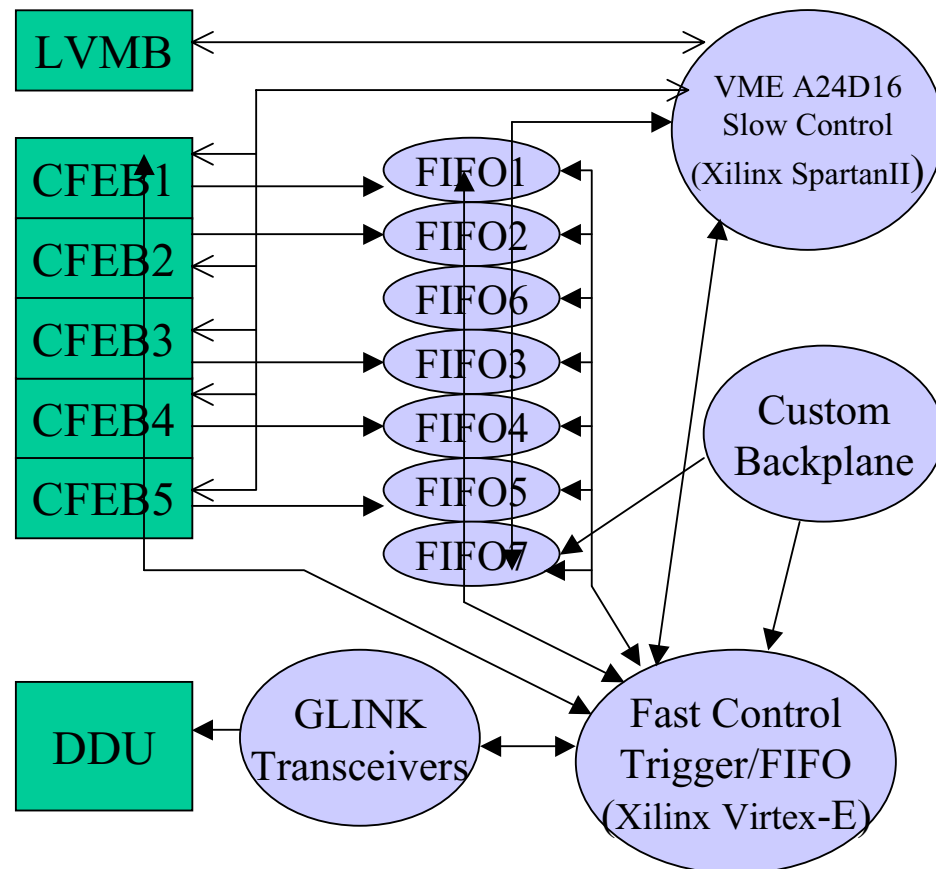


# DMB-01

## Prototype II – Similar Architecture as DMB-99

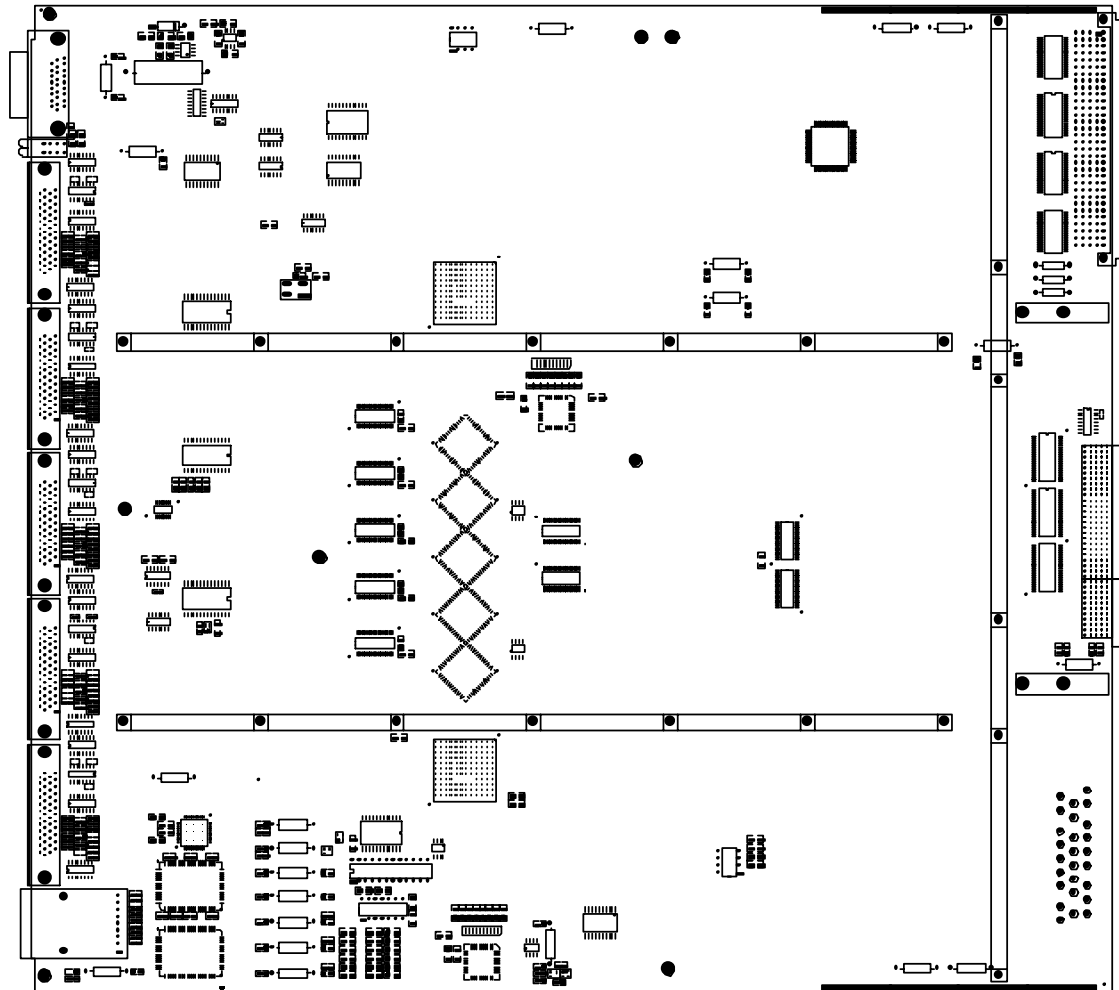
- VME custom backplane signals added
- VME Slow control (XILINX Spartan II) added
- 3 FPGA/CPLD consolidated into 1 XILINX Virtex E for fast control
- Interface for low voltage monitoring added
- HP-GLINK TI-TLK2501  
(Keep comp. with old DDU;  
lower power, cheaper  
chips, 8b/10b  
encoding/decoding, ... )

## Block Diagram of DMB





# ***DMB-01 Layout***



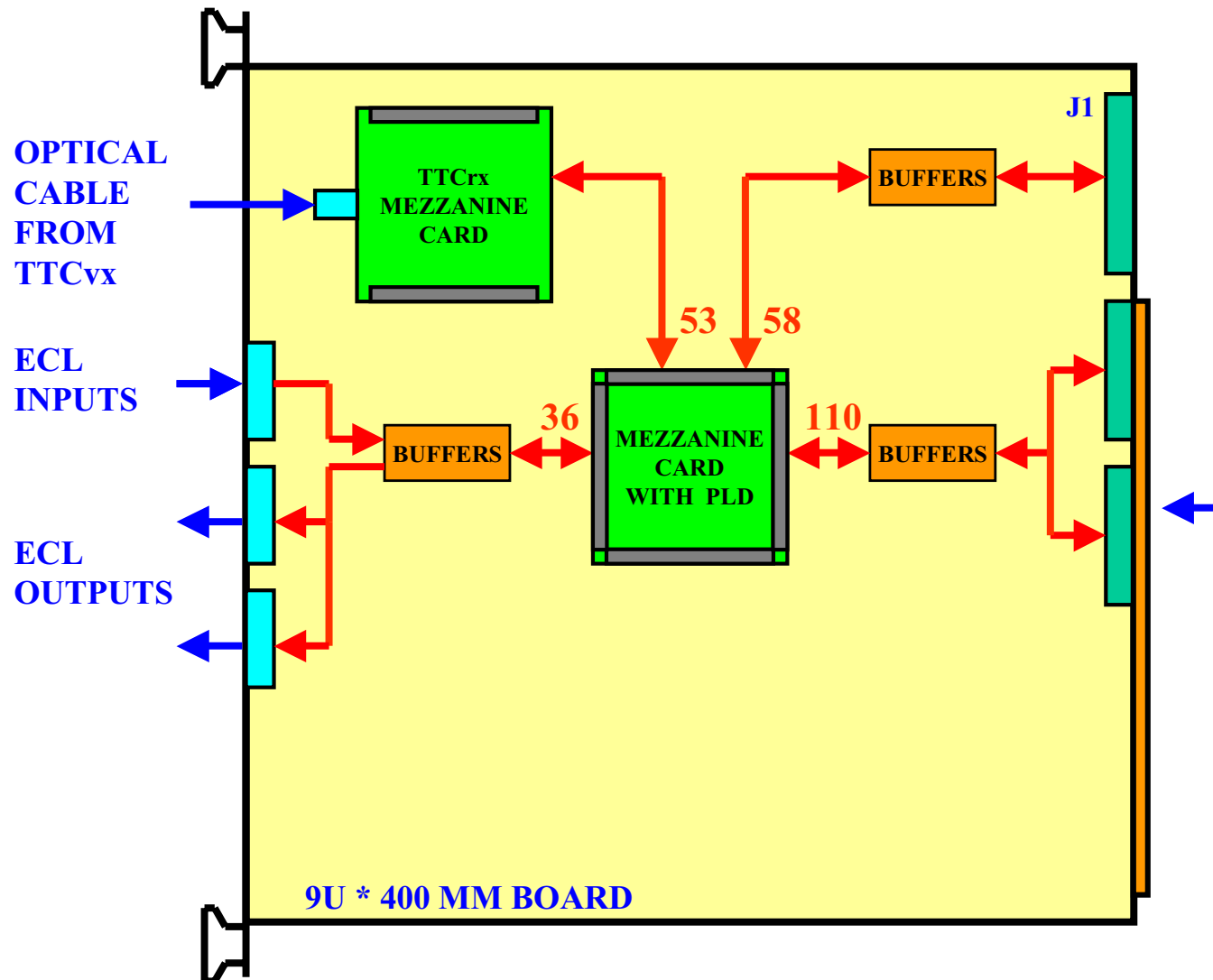


# CCB-01

	CCB-99	CCB-01
<b>Connections to TMB, DMB, MPC</b>		
<b>Interface logic</b>	<b>Cables</b>	<b>Backplane</b>
<b>Number of serviced modules</b>	<b>LVDS</b>	<b>LVDS + GTLP</b>
<b>Total number of signals to modules</b>	<b>6</b>	<b>19</b>
<b>Interface to TTC</b>	<b>24 (out)</b>	<b>129 (in/out)</b>
<b>Fast control bus signals</b>	<b>Old TTCrx</b>	<b>New TTCrx</b>
<b>Reloading protocol signals</b>	<b>no</b>	<b>yes</b>
<b>Special purpose bus signals</b>	<b>no</b>	<b>yes</b>
<b>FPGA Technology</b>	<b>no</b>	<b>yes</b>
	<b>Altera 10KA</b>	<b>Altera 10KA</b>
		<b>(on mezzanine card)</b>



## CCB-01 Block Diagram





# ***Conclusions***

- **Performance requirements met for CFEB, AFEB.**
- **Tests on radiation tolerance, magnetic field tolerance, spark protection done successfully.**
- **Production of CFEB and AFEB started (2/01). It is on-schedule and under budget (CFEB).**
- **ALCT board has been redesigned, largely motivated by radiation test result. Pre-production boards expected in ~10/01.**
- **LVDB Production start when ST regulators are delivered (7/01?)**
- **Off-chamber electronics: Good progresses made on next round of prototype boards and on VME custom backplane.**